HD63486

Graphic Video Attribute Controller (GVAC)

Description

The HD63486 LSI belongs to the ACRTC (advanced CRT controller) family. It converts frame buffer data to serial video signals. It contains a shift register for parallel-to-serial conversion and the peripheral video control circuits necessary to generate high-speed video signals.

The programmable bit length of the shift register makes the GVAC suitable for multicolor graphics and monochrome grey scale applications. Additionally, multiple GVACs can be operated in parallel to further expand the field of applications. The GVAC's functions include horizontal smooth scrolling and horizontal zoom using control signals from the GMIC (graphic memory interface controller). Using the Hi-BiCMOS process, the HD63486 achieves high-speed video signal generation with low power dissipation.

Features

- Internal shift register for video signal control, programmable as:
  - —Four 8-bit shift registers
  - —Two 16-bit shift registers
  - —One 32-bit shift register
- High speed video signal generation (64 MHz dot rate)
- Multiple GVAC parallel operation
- Internal bidirectional data bus buffer for frame buffers
- Zooming and horizontal smooth scrolling (requires GMIC signals or equivalent)
- Direct ACRTC interface
- TTL-compatible input/output
- Single + 5 V power supply
- Low power dissipation

Type of Products

Part No.	Speed	Package
HD63486PS32	32 MHz	64-pin Plastic Shrink DIP
HD63486PS48	48 MHz	(DP-64S)
HD63486PS64	64 MHz	
HD63486CP32	32 MHz	68-pin PLCC
HD63486CP48	48 MHz	(CP-68)
HD63486CP64	64 MHz	

Pin Description

Figure 1 shows the pin arrangement for the 64-pin plastic shrink-type DIP and the 68-pin PLCC packages. Table 1 describes the pins.

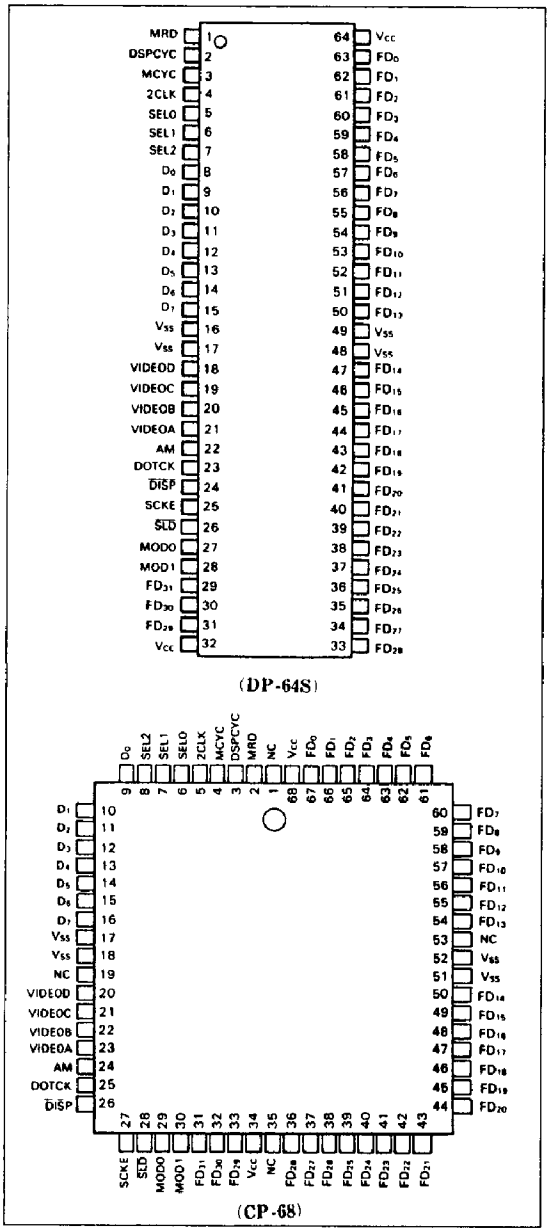

Figure 1. Pin Arrangement

Power Supply (V_{CC}, V_{SS})

V_{SS} and V_{CC} are the GVAC power supply pins. V_{CC} pins are + 5 V ± 5% supply pins. V_{SS} are the ground pins. Be sure to connect all four V_{SS} pins to ground and both V_{CC} pins to the power supply.

ACRTC Signals

Clock (2CLK): The 2CLK input must be the same as the 2CLK input to the ACRTC. It is usually supplied by the GMIC 2CLKOUT output. 2CLK is used for data transfer between the ACRTC and frame buffers and as a timing signal for display data input.

Memory Cycle (MCYC): The MCYC input specifies frame buffer access by the ACRTC. It must be low when the ACRTC is in address cycle, and high when the ACRTC is in data cycle. MCYC controls the data buffers. It is usually supplied by the ACRTC's MCYC output.

Memory Read (MRD): The MRD input controls the direction of transfers between the ACRTC and frame buffers. When MRD is high, the GVACs transfer data from the frame buffers to the ACRTC. When MRD is low, the GVACs transfer data from the ACRTC to the frame buffers. MRD must be held high during a display read data cycle. Only during a display cycle for superimposed screen data (dual access mode 1) does the ACRTC input MRD low. This signal is usually supplied by the MRD output.

Display ($\overline{DISP}$): The $\overline{DISP}$ input is a composite signal indicating the screen's horizontal and vertical display period. Display timing output ($\overline{DISP1}$) is input when the ACRTC's DSP (display signal control) bit is set to 1. For superimposed display (dual access mode 1), $\overline{DISP1}$ must be input to a GVAC for background screens, while $\overline{DISP2}$ must be input the window screen from the ACRTC.

Data Bus (D_7-D_0): D_7-D_0 are the 8-bit data input/output for data transfer between the ACRTC and frame buffers. Usually, D_7-D_0 are connected to 8 bits of the memory address data bus (MAD_{18}-MAD_0) according to the operation mode selected by the MOD1, MOD0 inputs.

Table 1. Pin Description

Signal	Pin Number DIP-64	Pin Number PLCC-68	I/O	Description
V_{CC}	32, 64	34, 68		+5 V power supply
V_{SS}	16, 17, 48, 49	17, 18, 51, 52		Ground
2CLK	4	5	I	Clock
MCYC	3	4	I	Memory Cycle
MRD	1	2	I	Memory Read
$\overline{DISP}$	24	26	I	Display
D_7-D_0	15-8	16-9	I/O	Data Bus
MOD1, MOD0	28, 27	30, 29	I	Operation Mode
AM	22	24	I	Access Mode
DSPCYC	2	3	I	Display Cycle
SEL2-SEL0	7-5	8-6	I	Select
SCKE	25	27	I	Shift Clock Enable
$\overline{SLD}$	26	28	I	Shift Load
FD_{31}-FD_0	29-31, 33-47, 50-63	31-33, 36-50, 54-67	I/O	Frame Buffer Data
DOTCK	23	25	I	Dot Clock
VIDEOA-VIDEOD	21-18	23-20	O	Video Outputs

For systems with a superimpose function, SCKE must be held high for the superimposed window's GVAC (AM input high).

Shift Load ($\overline{SLD}$): The $\overline{SLD}$ input specifies the timing in which display data temporarily stored in the GVACs is supplied to the shift register. $\overline{SLD}$ is asserted for one period of the dot clock. Horizontal scrolling is implemented by shifting $\overline{SLD}$ on a dot clock basis during a single display cycle. $\overline{SLD}$ must be asserted once during each display cycle (shift length). $\overline{SLD}$ is usually input from the GMIC $\overline{SLDB}$ output for background screen GVACs (AM input low), and $\overline{SLDW}$ for window screen GVACs (AM input high).

Frame Buffer Data (FD_{31}-FD_0)

The 32-bit FD_{31}-FD_0 frame buffer data I/O bus transfers data between the ACRTC and frame buffers and inputs display data from the frame buffers. The 32 bits arj read simultaneounly from the frame buffer, and FD_{31}-FD_0 can be directly connected to the frame buffer data I/O pins.

CRT Display Interface

Dot Clock (DOTCK): The DOTCK input is the basic video signal generating clock. The DOTCK frequency is determined by the CRT horizontal resolution (pixel count) and the horizontal scan display period. This clock is usually the same signal applied to the GMIC DOTCK input.

Video Outputs (VIDEOA-VIDEOD): VIDEOA -VIDEOD are the four bits output from the GVAC's parallel-to-serial conversion shift register. They are supplied during a display period specified by the display signal ($\overline{DISP}$). Which outputs are usable depends on the operation mode (MOD1, MOD0) input. Table 3 shows the usable video signals and corresponding MOD1 and MOD0 signals.

Table 3. Operation Mode and Video Outputs

Mode		Video Output				Bits/	
MOD1	MOD0	VIDEOA	VIDEOB	VIDEOC	VIDEOD	Pixel	Shift Length
0	0	Avail	Not avail	Avail	Not avail	4	16
0	1	Avail	Not avail	Not avail	Not avail	4	32
1	0	Avail	Avail	Avail	Avail	8	8
1	1	Avail	Not avail	Avail	Not avail	8	16

Functional Description

Figure 2 is a block diagram of the GVAC.

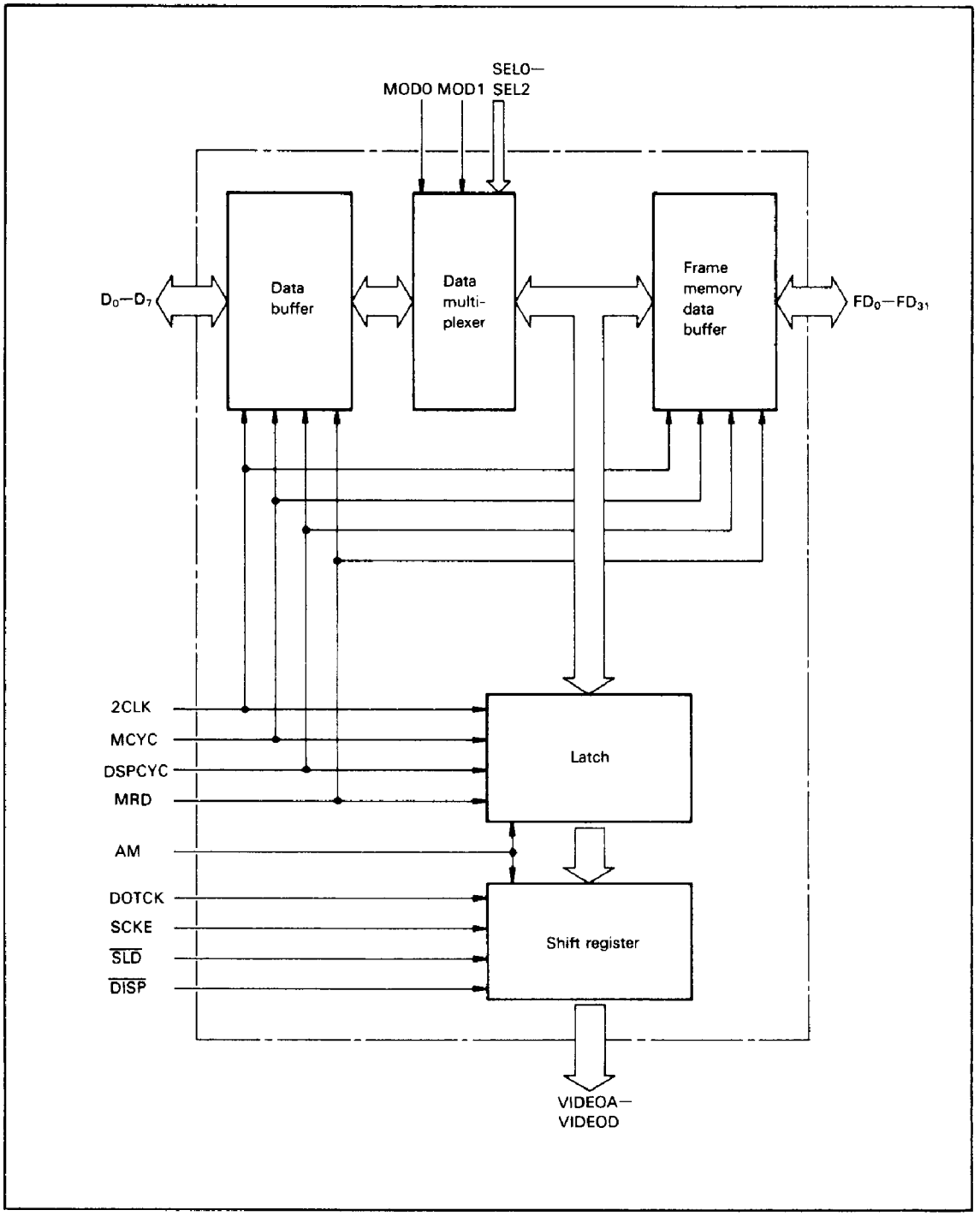

Figure 2. GVAC Block Diagram

Frame Memory Data Buffer

The 32-bit bidirectional frame memory data buffer consists of input and output buffers to transfer data to and from the frame buffers in response to data transfer requests from the ACRTC.

The three-state output buffer is enabled only during a memory write cycle by memory cycle (MCYC) and memory read (MRD) signals from the ACRTC, and display cycle (DSPCYC) from the GMIC. A 32-bit output buffer to be enabled is selected by select signals (SEL2-SEL0) from the GMIC and the operation mode (MOD1, MOD0) set externally.

The input buffer reads data from the frame buffers.

Data Buffers

The 8-bit input/output buffer transfers data between the ACRTC and frame buffers.

The output buffer is a three-state buffer which is enabled during a frame buffer read cycle by memory cycle (MCYC) and memory read (MRD) signals from the ACRTC, and display cycle (DSPCYC) from the GMIC.

The input buffer supplies drawing data from the ACRTC to the frame buffers.

Data Multiplexer

The data multiplexer is a direct connection between the frame buffers and the data buffer's data bus which leads to the ACRTC's and frame buffer's data bus. The bus connection in controlled by select signals (SEL2-SEL0) and the operation mode (MOD1, MOD0) set externally to enable transfer between the ACRTC and frame buffers.

Latch

The latch recognizes a display data read cycle by memory cycle (MCYC) and memory read (MRD) signals from the ACRTC, and clock (2CLK) and display cycle (DSPCYC) from the GMIC, and the access mode (AM) input. During a display data read cycle, the latch temporarily stores 32-bit display data input from a frame memory data buffer. It sends the stored data to the shift register for parallel-to-serial conversion.

Shift Register

The 32-bit shift register performs parallel-to-serial conversion on display data stored in the latch to provide video signal output. When the latch receives the shift load ($\overline{SLDB}$, $\overline{SLDW}$) and shift clock enable (SCKE) signals from the GMIC, it feeds the display data it has stored to the shift register. The shift register supplies one bit of display data every dot clock cycle while SCKE is asserted. When the ACRTC's display cycle signal (DISP) is negated, the shift register does not output a video signal.

When the GMIC shifts the timing of the shift load ($\overline{SLDB}$, $\overline{SLDW}$) output on a dot clock basis, the GVAC performs horizontal smooth scrolling. When the GMIC extends the shift clock enable signal (SCKE) based on the dot clock, it performs horizontal zoom.

System Description

Applications

The GVAC internal circuits perform three major functions:

- Converting parallel display data read from the frame buffers by the ACRTC to serial from and delivering them to the CRT as video signals
- Transferring data between the ACRTC and frame buffers
- Zooming and horizontal smooth scrolling according to signals from the GMIC

Furthermore, the GVACs' operation mode can be set according to the ACRTC's operation mode by the program input signals. This programmability makes the GVAC suitable for a wide range of applications, from slow, small systems to fast, large systems. It also permits the GVACs to accommodate system specification changes.

Figure 3 shows a graphic system configuration using an ACRTC, GMIC and GVACs. With the GMIC used for interfacing with frame buffers and the GVACs generating the video signals, a flexible, high-performance graphic system is constructed with a minimum number of parts.

System Configuration

The system example in figure 3 uses two GVACs, but the number of GVACs can be varied to meet different CRT resolution and color per pixel (or grey scale) applications.

The GVACs recognize a display data read cycle by decoding ACRTC output signals such as memory cycle (MCYC) and memory read (MRD) and GMIC output signals such as display cycle (DSPCYC). In the display data read cycle, the GVACs latch display data from the frame buffers. They pass the display data to the internal shift register for parallel-to-serial conversion when they receive the shift load signal ($\overline{SLDB}$ or $\overline{SLDW}$) from

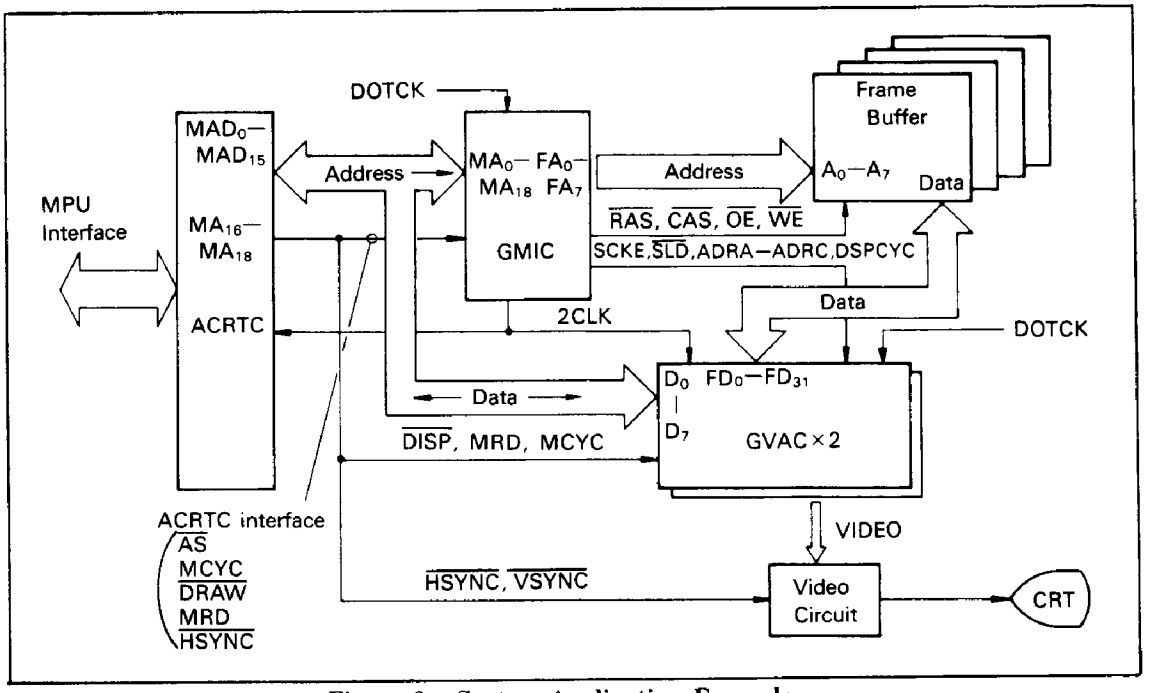

Figure 3. System Application Example

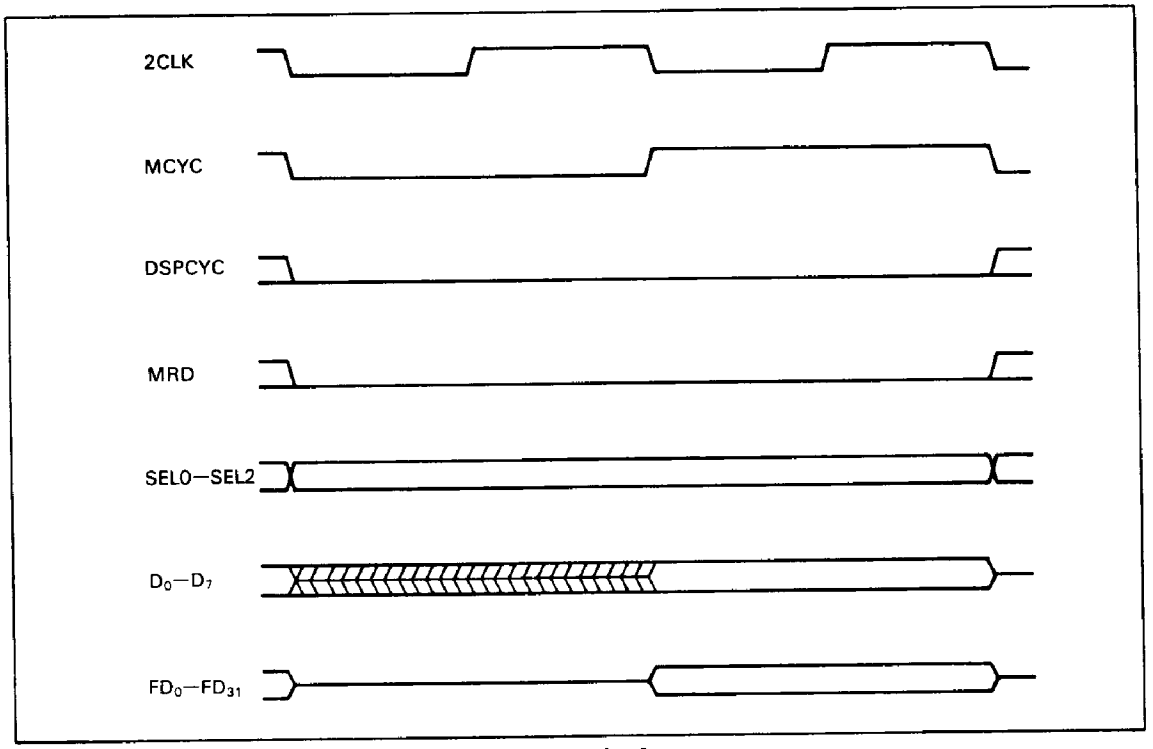

Figure 4. Drawing Write Cycle
(ACRTC [MAD] → [D] GVAC [FD] → Frame buffers)

Drawing Read Cycle : The GVACs recognize a drawing read cycle when DSPCYC is low and MRD is high. Figure 5 shows the timing for a drawing read cycle.

When MCYC is high during this cycle, the GVACs enable the data buffer (D_7-D_0) for the ACRTC and output a word from the frame buffers selected by the operation mode (MOD1, MOD0) inputs and the select signals (SEL2-SEL0) from the GMIC. Table 4 shows the connections between FD and D pins when MOD1 and MOD0 are set to 00. When SEL2-SEL0 are set to 000, data from FD_0-FD_3 from the ACRTC are output to D_0-D_3, data from FD_{16}-FD_{19} are output to D_4-D_7, and the other FD pins cannot be used. Table 5-7 show the relation of D to FD in other modes. D pins which are not connected (NC) must be held high by pull-up resistors.

GVAC Connections

The GVACs allow three shift modes to be selected externally through the operation mode pins (MOD1, MOD0). The number of GVACs used is determined by the selected shift mode, graphic bit mode (GBM) which sets ACRTC bits per pixel, and graphic address increment mode (GAI) which sets the number of display data bits read from the frame buffers simultaneously (table 8).

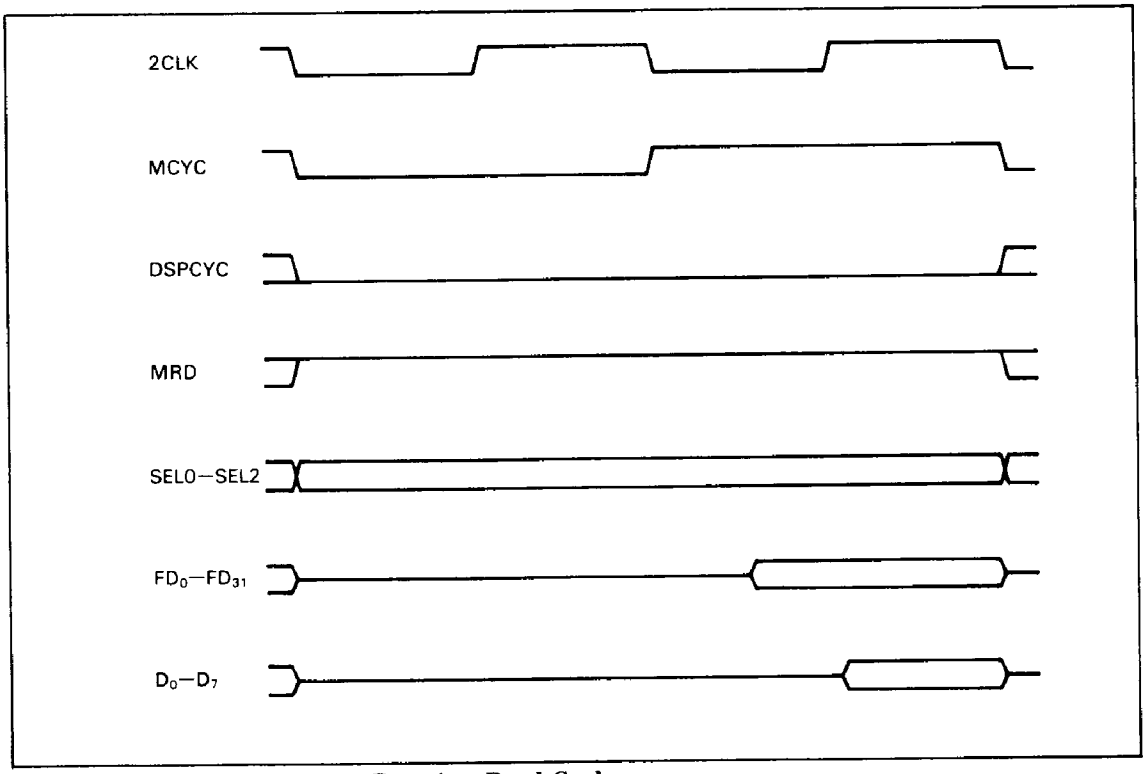

Figure 5. Drawing Read Cycle
(Frame buffer → [FD] GVAC [D] → ACRTC [MAD])

Table 8. Number of GVACs

ACRTC GBM 10 9 8	ACRTC GAI 6 5 4	GVAC MOD 1 0	Bits/ Pixel	Words Read	Bits Read	Shift Length	Number of GVACs
0 0 0	0 0 0	0 0	1	1	16	16	1 (2)*
	0 0 1	0 1	1	2	32	32	1 (2)*
0 0 1	0 0 0	1 0	2	1	16	8	1 (2)*
	0 0 1	0 0	2	2	32	16	1 (2)*
	0 1 0	0 1	2	4	64	32	2 (4)*
0 1 0	0 0 1	1 0	4	2	32	8	1 (2)*
	0 1 0	0 0	4	4	64	16	2 (4)
	0 1 1	0 1	4	8	128	32	4 (8)
0 1 1	0 1 0	1 0	8	4	64	8	2 (4)
	0 1 1	1 1	8	8	128	16	4 (8)
1 0 0	0 1 1	1 0	16	8	128	8	4 (8)*

Notes: 1. *Indicates that data transfers between frame buffers and the ACRTC requires external circuits since the GVACs to ACRTC data transfer function cannot be used directly.
2. Parenthesized values are the number of GVACs required for superimpose mode (dual access mode 1) applications.

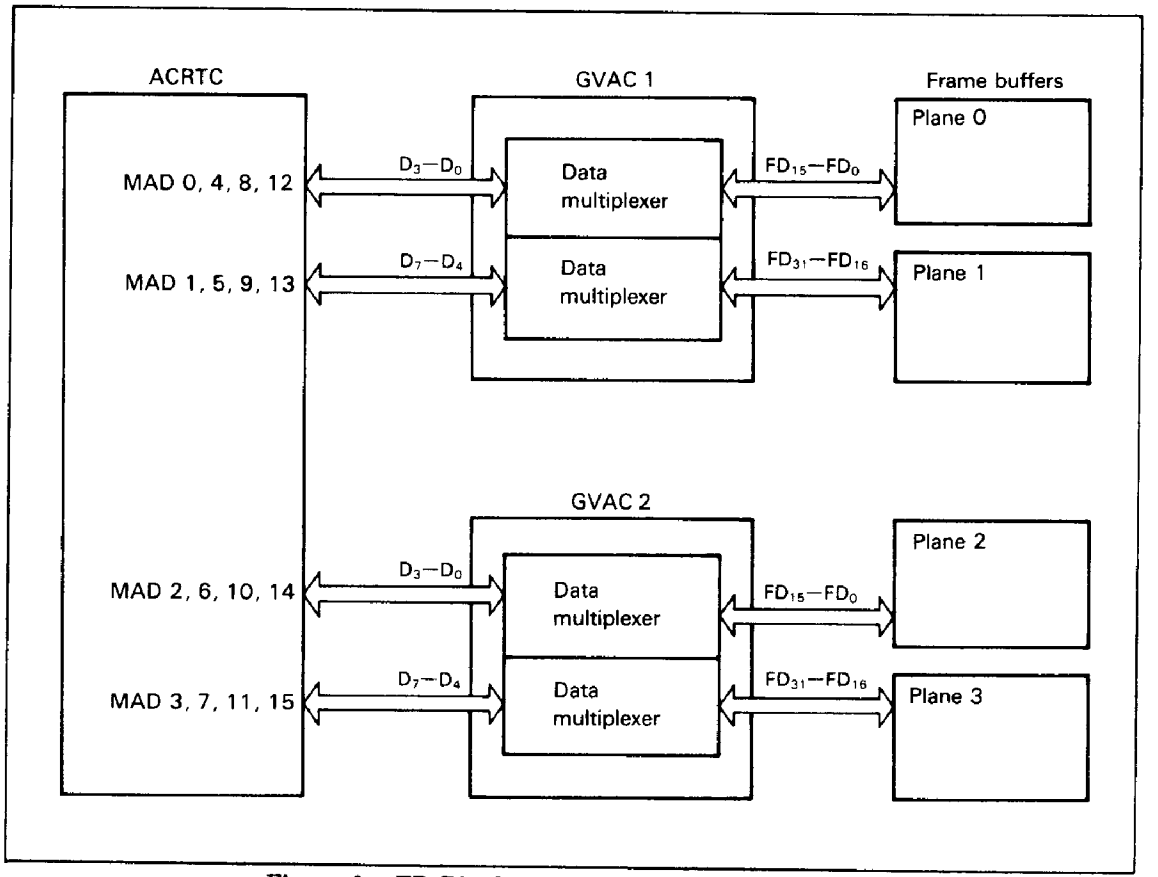

Figure 6. FD Pin Connection (MOD1, MOD0 = 00)

Data Connections

Figure 6 illustrates the data pin connection with MOD1, MOD0 set to 00. In this mode, one pixel consists of 4 bits, and four words (64 bits) are read from the frame buffers at one time.

ACRTC and GVAC Connection

ACRTC Display Data Bit Configuration : The ACRTC handles display data on a pixel basis, the ACRTC's mimimum unit. The ACRTC transfers data on a word (16-bit) basis. One memory word can consist of one or more pixels. The ACRTC's graphic bit mode (GBM) selects one of five types of pixel count. The GVACs directly support data transfers of 4 bits or 8 bits per pixel. In 4 bit/pixel mode, 16 colors or shades of grey can be implemented at one time. In 8 bit/pixel mode, 256 colors or 256 shades of grey can be realized. Figure 7 shows pixel data processed by the ACRTC depending on operation mode pin 1 (MOD1). For details on the graphic bit mode, see the ACRTC User's Manual, 5.5.6 Graphic Bit Mode.

GVAC and Graphic Data : The GVACs must be connected to handle data on a one-pixel bit plane basis. Table 9 shows the relationship between operation mode 1 (MOD1), pixel number, bit plane number, and ACRTC data.

Connection Between GVACs and ACRTC : The connection to the ACRTC depends on the operation mode (MOD1, MOD0). Table 10 shows the connection with MOD1, MOD0 = 00. In this mode, each pixel is four bits. GVAC1 handles bit planes 0 and 1, and GVAC2 handles bit planes 2 and3. The connection between the ACRTC and GVACs is determined by bit plane number and pixel number for one word from the ACRTC. In table 9, for example, ACRTC pin MAD0 corresponds to bit plane 0 for pixel number 0. From table 10, therefore, bit plane number 0 for GVAC1 is connected to pin D_0 for pixel number 1. Connection to the ACRTC in other modes are shown in table 11-13.

Table 9. Pixel Number and Plane Number

		MAD															
MOD1	**ACRTC**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Pixel No.	3				2				1				0			
	Bit Plane No.	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
1	Pixel No.	1											0				
	Bit Plane No.	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

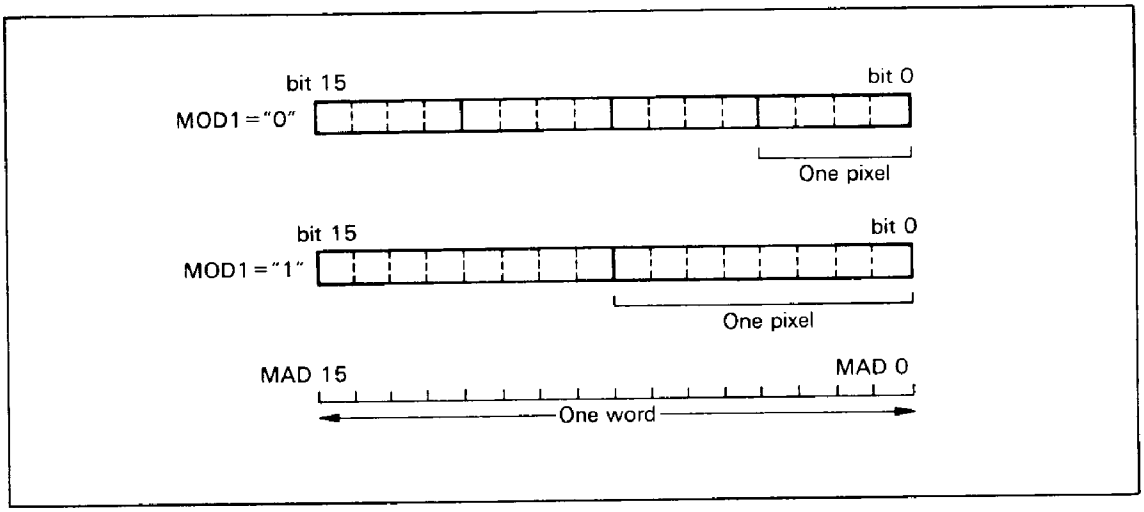

Figure 7. Pixel Data and MOD1

Table 10. ACRTC and GVAC Pin Connection, MOD1, MOD0 = 00 (4 Bits/Pixel, 16-Bit Shift Mode)

	MAD															
Connection	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Pin Connection	D_7	D_3	D_7	D_3	D_6	D_6	D_6	D_2	D_5	D_1	D_5	D_1	D_4	D_0	D_4	D_0
GVAC	2	2	1	1	2	2	1	1	2	2	1	1	2	2	1	1
Pixel Number	3	3	3	3	2	2	2	2	1	1	1	1	0	0	0	0
Bit Plane	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
Frame Buffer Pixel Number	3	3	3	3	2	2	2	2	1	1	1	1	0	0	0	0

Table 11. ACRTC and GVAC Pin Connection, MOD1, MOD0 = 01 (4 Bits/Pixel, 32-Bit Shift Mode)

	MAD															
Connection	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Pin Connection	D_3	D_3	D_3	D_3	D_2	D_2	D_2	D_2	D_1	D_1	D_1	D_1	D_0	D_0	D_0	D_0
GVAC	4	3	2	1	4	3	2	1	4	3	2	1	4	3	2	1
Pixel Number	3	3	3	3	2	2	2	2	1	1	1	1	0	0	0	0
Bit Plane	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
Frame Buffer Pixel Number	3	3	3	3	2	2	2	2	1	1	1	1	0	0	0	0

Note: D_7-D_4 cannot used in this mode

Table 12. ACRTC and GVAC Pin Connection, MOD1, MOD0 = 10 (8 Bits/Pixel, 8-Bit Shift Mode)

	MAD															
Connection	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Pin Connection	D_7	D_5	D_3	D_1	D_7	D_5	D_3	D_1	D_6	D_4	D_2	D_0	D_6	D_4	D_2	D_0
GVAC	2	2	2	2	1	1	1	1	2	2	2	2	1	1	1	1
Pixel Number	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Bit Plane	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Frame Buffer Pixel Number	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Table 13. ACRTC and GVAC Pin Connection, MOD1, MOD0 = 11 (8-Bits/Pixel, 16-Bit Shift Mode)

	MAD															
Connection	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Pin Connection	D_5	D_1	D_5	D_1	D_5	D_1	D_5	D_1	D_4	D_0	D_4	D_0	D_4	D_0	D_4	D_0
GVAC	4	4	3	3	2	2	1	1	4	4	3	3	2	2	1	1
Pixel Number	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Bit Plane	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Frame Buffer Pixel Number	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Note: D_7, D_6, D_3, D_2 cannot be used in this mode

Connection Between Frame Buffers and GVACs: Like the connection to the ACRTC, the data connection to the frame buffers is made on the basis of a bit plane consisting of one word, sequentially from the lower pixel address. Table 14 shows pixel number for the frame buffer's word (16 bits) vs bit plane number for one pixel in relation to operation mode 1 (MOD1).

Table 15 shows the connection between the GVACs and frame buffers with MOD1, MOD0 = 00. In this mode, the ACRTC's graphic address increment (GA1) is set to +4 mode, and 4-word data is simultaneously read from the frame buffers. GVAC1 handles bit planes 0 and 1, and GVAC2 handles bit planes 2 and 3. For example, pin FD_0 of GVAC1 is connected to a data pin of pixel number 0 of the n + 0 address of bit plane number 0. Connections in other modes are shown in tables 16–18.

Table 14. One-Word Frame Buffer Pixel Number and Corresponding Bit Plame Number

		One word of frame buffer															
		Pixel Number															
MOD1		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Bit Plane No.	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
	Pixel No.	3				2				1				0			
1	Bit Plane No.	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Pixel No.	1								0							

Table 15. GVAC and Frame Buffer Pin Connection, MOD1, MOD0 = 00 (4 Bits Pixel, 16-Bit Shift Mode)

GVAC		FD31	FD30	FD29	FD28	FD27	FD26	FD25	FD24	FD23	FD22	FD21	FD20	FD19	FD18	FD17	FD16	FD15	FD14	FD13	FD12	FD11	FD10	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
1	Bit Plane No.	1																						0									
	Pixel No.	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
	Word Address	n+3				n+2				n+1				n+0				n+3				n+2				n+1				n+0			
2	Bit Plane No.	3																						2									
	Pixel No.	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
	Word Address	n+3				n+2				n+1				n+0				n+3				n+2				n+1				n+0			

Table 16. GVAC and Frame Buffer Pin Connection, MOD1, MOD0 = 01 (4 Bits/Pixel, 32-Bit Shift Mode)

GVAC		FD31	FD30	FD29	FD28	FD27	FD26	FD25	FD24	FD23	FD22	FD21	FD20	FD19	FD18	FD17	FD16	FD15	FD14	FD13	FD12	FD11	FD10	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
1	Bit Plane No.	0																															
	Pixel No.	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
	Word Address	n+7				n+6				n+5				n+4				n+3				n+2				n+1				n+0			
2	Bit Plane No.	1																															
	Pixel No.	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
	Word Address	n+7				n+6				n+5				n+4				n+3				n+2				n+1				n+0			
3	Bit Plane No.	2																															
	Pixel No.	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
	Word Address	n+7				n+6				n+5				n+4				n+3				n+2				n+1				n+0			
4	Bit Plane No.	3																															
	Pixel No.	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
	Word Address	n+7				n+6				n+5				n+4				n+3				n+2				n+1				n+0			

Video Signal Generation

A GVAC performs parallel-to-serial conversion on 32-bit data read from frame buffers using the shift register, and produces 4-bit video signals (VIDEOA -VIDEOD).

The GVAC recognizes the cycle in which display data is read from frame buffers by memory cycle (MCYC) and memory read (MRD) signals from the ACRTC, display cycle (DSPCYC) from GMIC, and access mode (AM) signal externally set. The GVAC then latches 32-bit data supplied from FD_0-FD_{31} pins.

The latched display data is fed to the shift register on the falling edge of the dot clock (DOTCK) when the shift load ($\overline{SLD}$) input is asserted. This data is then shifted on the falling edge of the dot clock (DOTCK) when shift clock enable (SCKE) is asserted.

As seen in figure 8, 32-bit display data is output sequentially to four video signal pins one bit by one bit per dot clock (DOTCK).

- VIDEOA : 32 bits of FD_0-FD_{31}
- VIDEOB : 24 bits of FD_8-FD_{31}
- VIDEOC : 16 bits of FD_{16}-FD_{31}
- VIDEOD : 8 bits of FD_{24}-FD_{31}

Using the display timing signal ($\overline{DISP}$) from the ACRTC, 4-bit shift register output data can be masked. That is, while $\overline{DISP}$ is asserted, shift register output is provided as video signals, and while it is negated, shift register output is held low, and video signals are not output. The required number of dot cycles per display cycle is the same as the shift length value set by the operation mode (MOD1, MOD0).

Table 19 shows the dot clock cycle count per display cycle vs operation mode (MOD1, MOD0).

Table 17. GVAC and Frame Buffer Pin Connection, MOD1, MOD0 = 10 (8 Bits/Pixel, 8-Bit Shift Mode)

GVAC		FD31	FD30	FD29	FD28	FD27	FD26	FD25	FD24	FD23	FD22	FD21	FD20	FD19	FD18	FD17	FD16	FD15	FD14	FD13	FD12	FD11	FD10	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
1	Bit Plane No.	3								2								1								0							
	Pixel No.	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
	Word Address	n+3		n+2		n+1		n+0		n+3		n+2		n+1		n+0		n+3		n+2		n+1		n+0		n+3		n+2		n+1		n+0	
2	Bit Plane No.	7								6								5								4							
	Pixel No.	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
	Word Address	n+3		n+2		n+1		n+0		n+3		n+2		n+1		n+0		n+3		n+2		n+1		n+0		n+3		n+2		n+1		n+0	

Table 18. GVAC and Frame Buffer Pin Connection, MOD1, MOD0 = 11 (8 Bits/Pixel, 16-Bit Shift Mode)

GVAC		FD31	FD30	FD29	FD28	FD27	FD26	FD25	FD24	FD23	FD22	FD21	FD20	FD19	FD18	FD17	FD16	FD15	FD14	FD13	FD12	FD11	FD10	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
1	Bit Plane No.	1																0															
	Pixel No.	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
	Word Address	n+7		n+6		n+5		n+4		n+3		n+2		n+1		n+0		n+7		n+6		n+5		n+4		n+3		n+2		n+1		n+0	
2	Bit Plane No.	3																2															
	Pixel No.	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
	Word Address	n+7		n+6		n+5		n+4		n+3		n+2		n+1		n+0		n+7		n+6		n+5		n+4		n+3		n+2		n+1		n+0	
3	Bit Plane No.	5																4															
	Pixel No.	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
	Word Address	n+7		n+6		n+5		n+4		n+3		n+2		n+1		n+0		n+7		n+6		n+5		n+4		n+3		n+2		n+1		n+0	
4	Bit Plane No.	7																6															
	Pixel No.	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
	Word Address	n+7		n+6		n+5		n+4		n+3		n+2		n+1		n+0		n+7		n+6		n+5		n+4		n+3		n+2		n+1		n+0	

Figure 9, 10 and 11 show ACRTC frame buffer access vs video outputs in single access mode, dual access mode 0, and dual access mode 1. Superimposed display in dual access mode 1 requires that the window smooth scroll input (WSS) be high.

The GVAC provides display data output sequentially from four video outputs VIDEOA-VIDEOD synchronously with the dot clock while the shift clock enable input (SCKE) is asserted. Figure 12 shows the video signals output in GMIC divide-by-16 mode, GVAC's MOD1, MOD0 = 01, 32-bit shift mode. When shift load ($\overline{SLD}$) is asserted, display data (FD_{31}-FD_0) is sent to the shift register at the rising edge of the dot clock (DOTCK) to provide the sequential outputs. That is, video output A (VIDEOA) receives sequential outputs starting with FD_0, and the other video pins receive display data likewise. Figure 13 shows the video signals output in GMIC divide-by-4 mode, GVAC in 16-bit shift mode, and the ACRTC set in dual access mode 0. Figure 14 shows video outputs in the 8-bit shift mode, with the other conditions the same as in figure 13.

Table 19. Shift Length and Shift Clock

MOD1	MOD0	Shift Length	Dot Clocks/ Display Cycle
0	0	16	16
0	1	32	32
1	0	8	8
1	1	16	16

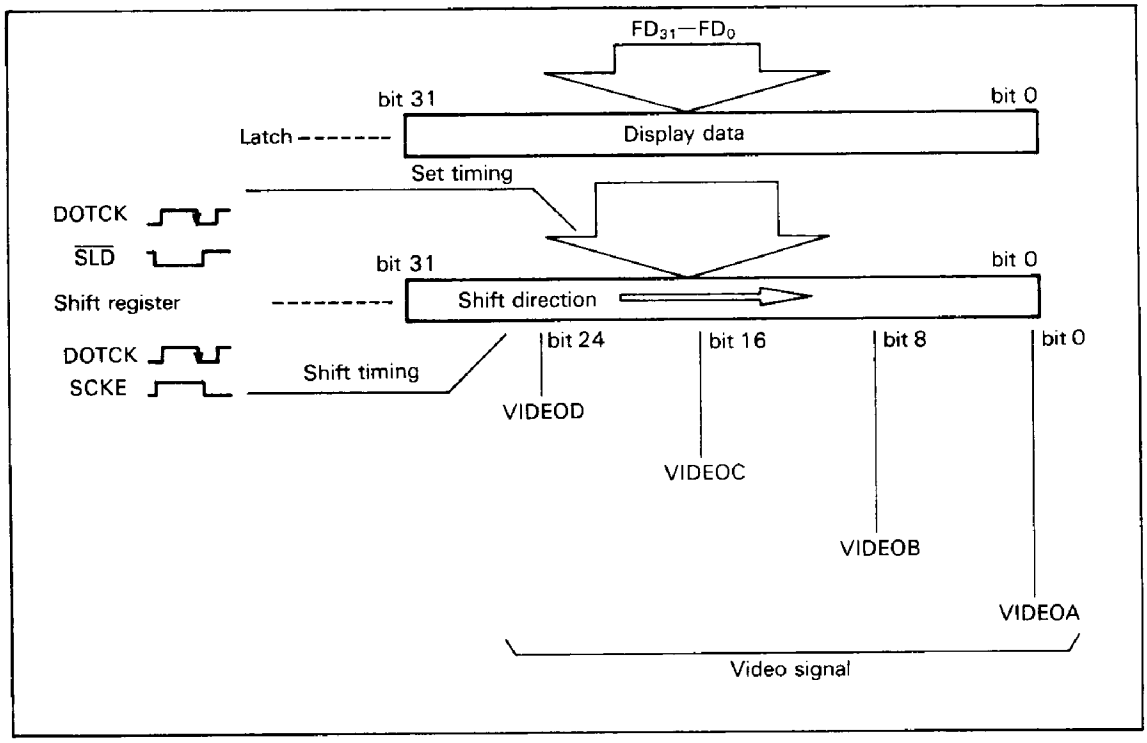

Figure 8. Video Signal Generation

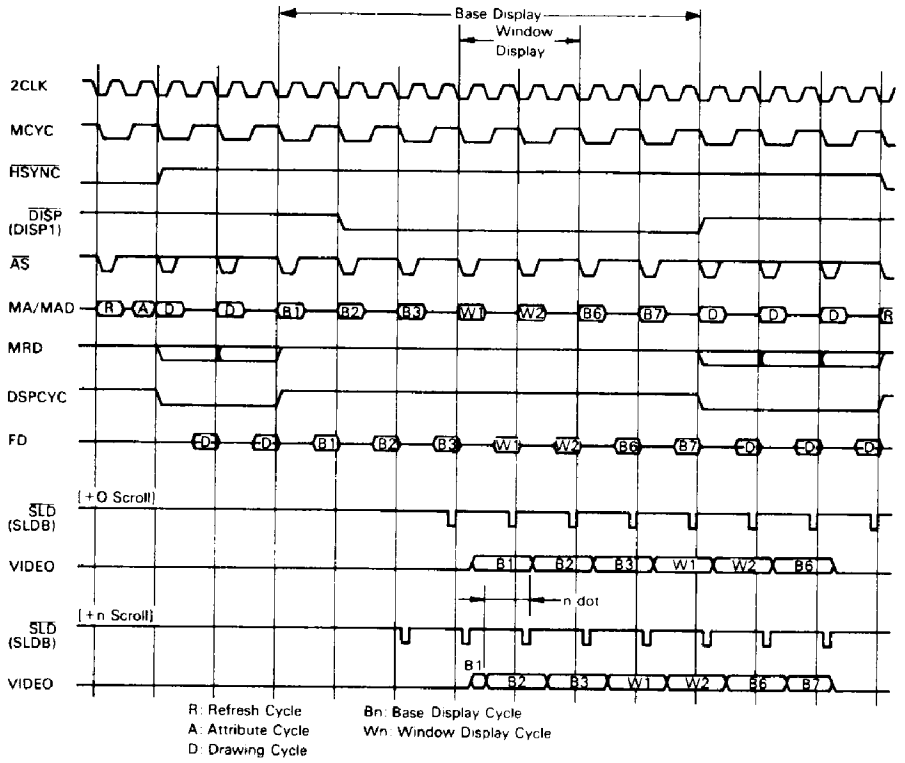

Figure 9. Video Output Timing (Single Access Mode)

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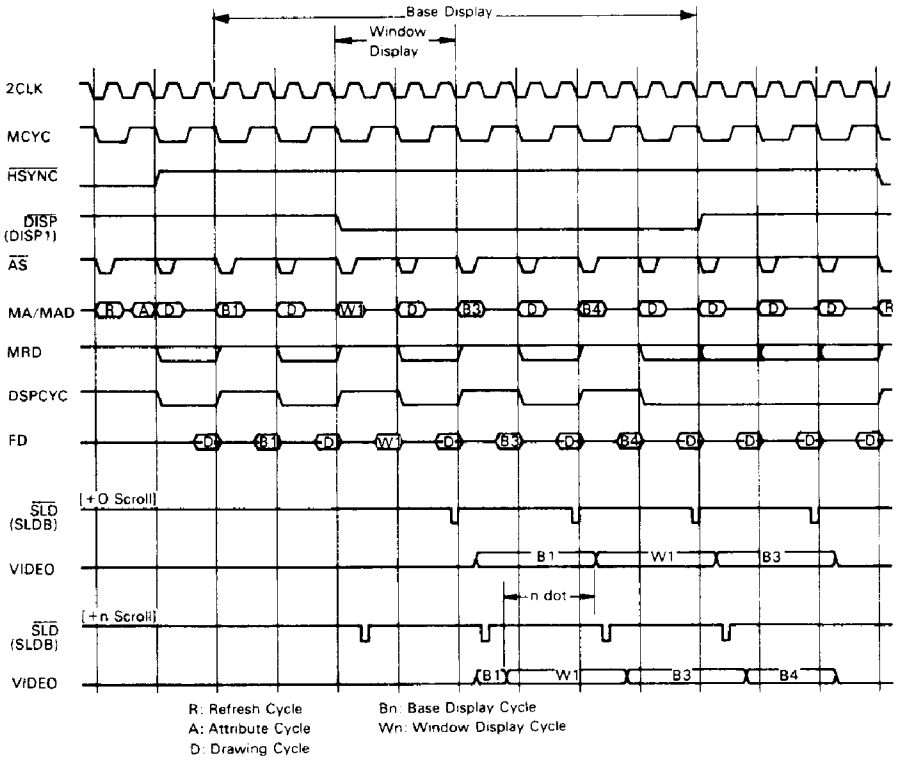

Figure 10. Video Output Timing (Dual Access Mode 0)

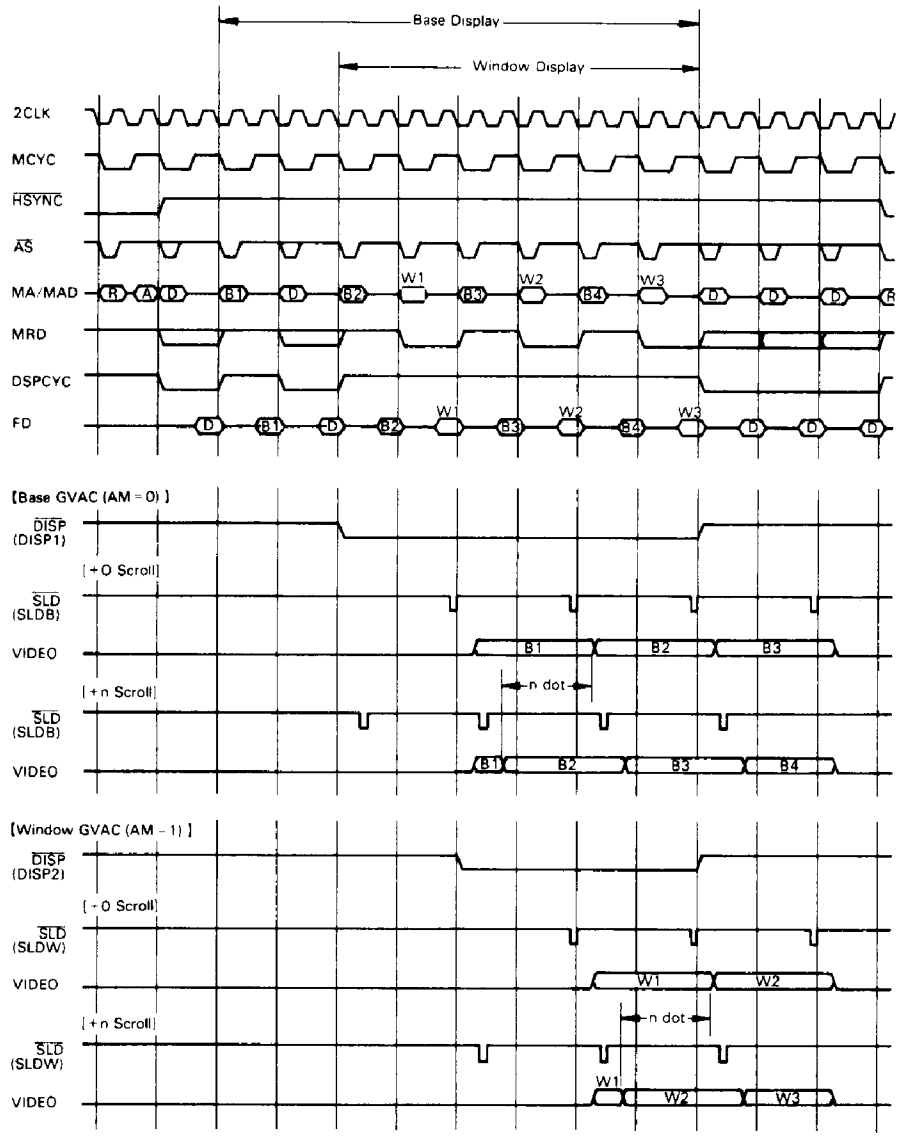

Figure 11. Video Output Timing (Dual Access Mode 1)

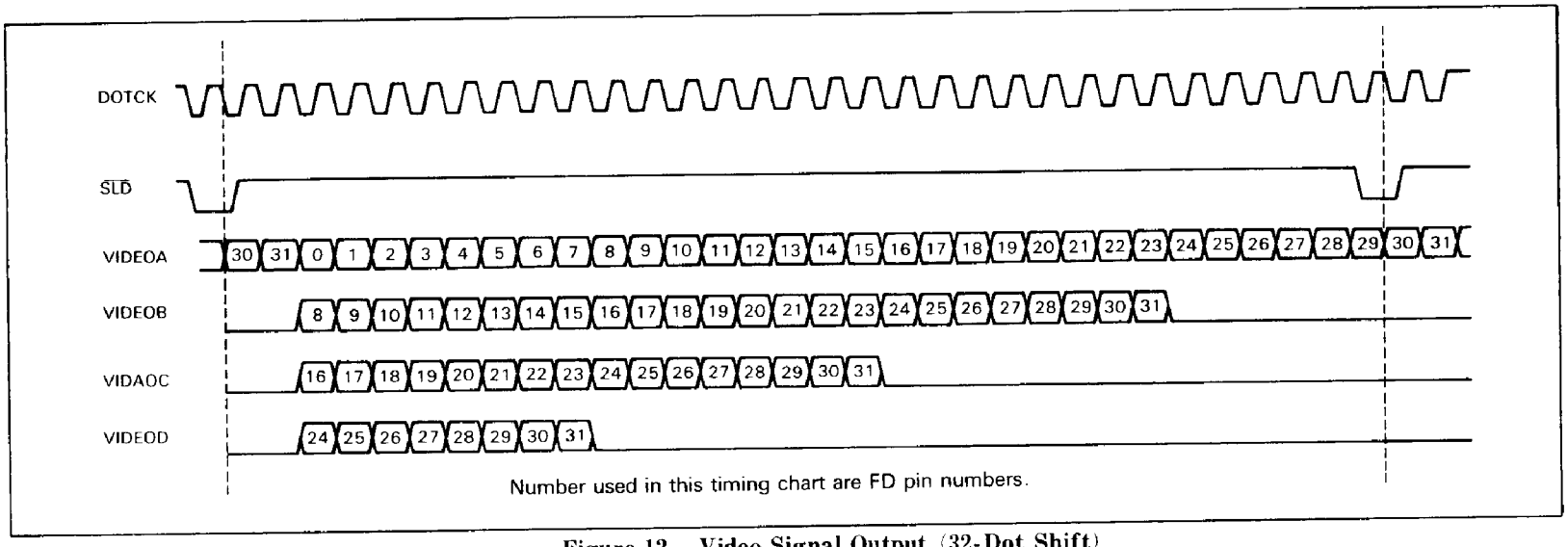

Figure 12. Video Signal Output (32-Dot Shift)

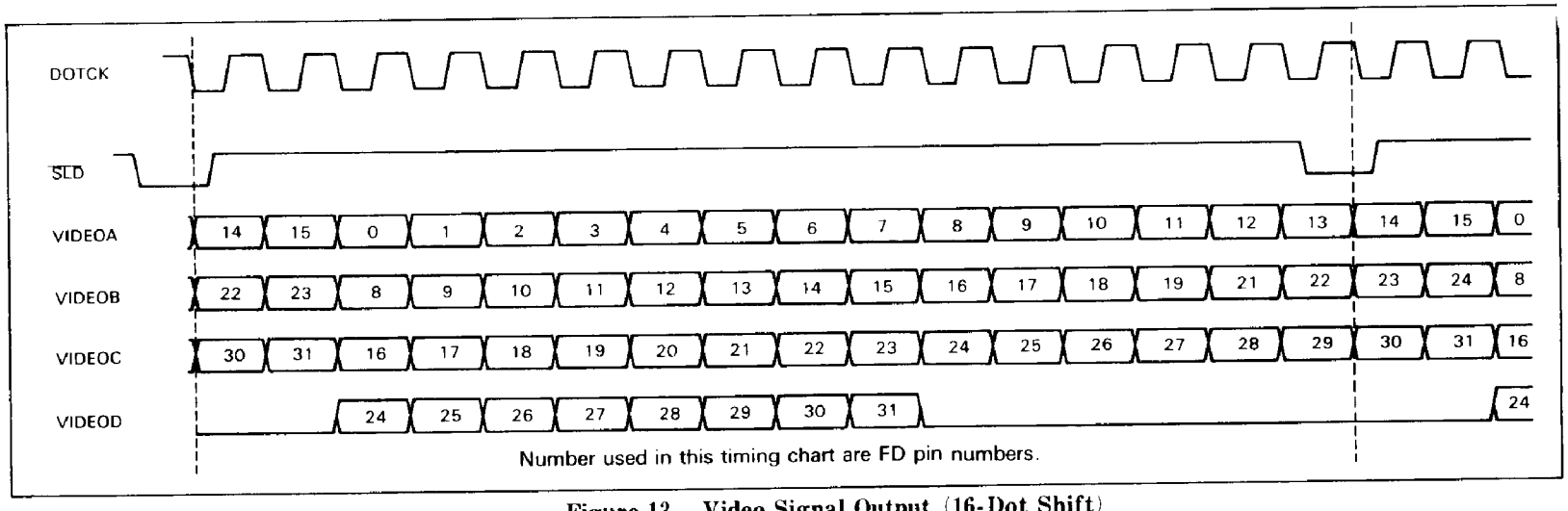

Figure 13. Video Signal Output (16-Dot Shift)

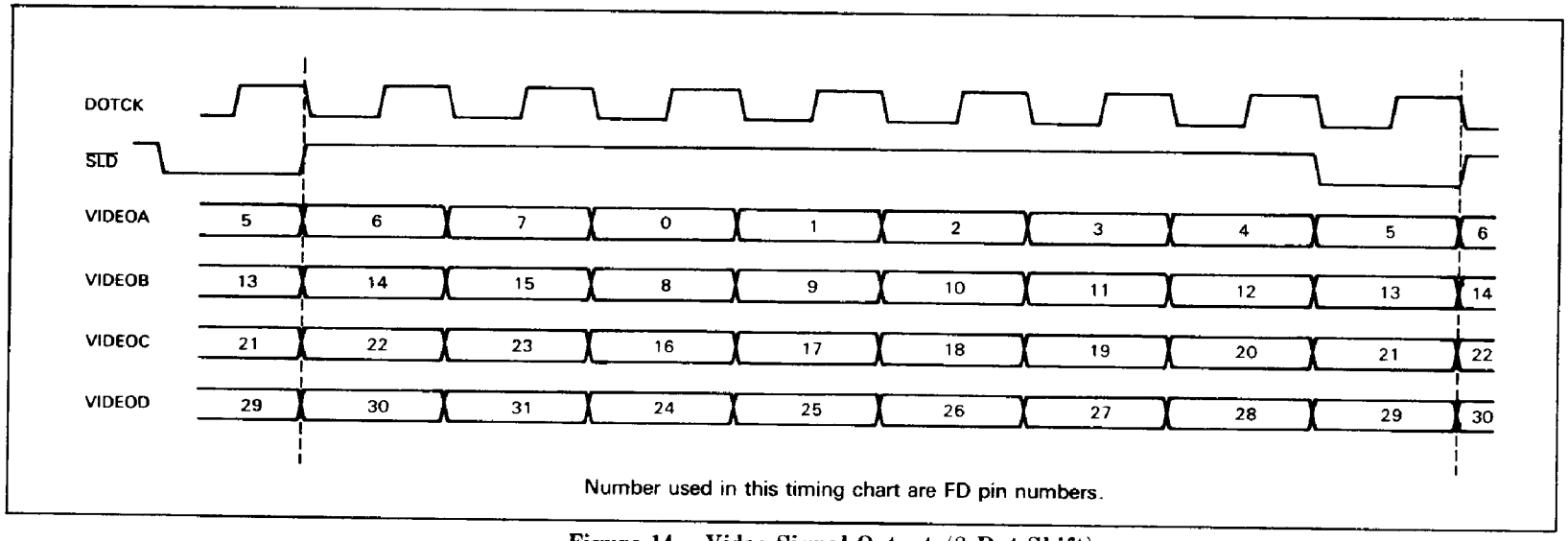

Figure 14. Video Signal Output (8-Dot Shift)

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Horizontal Smooth Scrolling

The GVAC performs horizontal smooth scrolling when the assertion period of the shift load signal ($\overline{SLD}$) is shifted on a dot clock basis. Table 20 shows horizontal smooth scroll dot count vs shift amount for the shift load signal ($\overline{SLD}$) in units of one dot clock cycle. Smooth scrolling is easily implemented by specifying the ACRTC's horizontal smooth scrolling dot (HSD) and sending the GMIC's $\overline{SLDB}/\overline{SLDW}$ signal to the GVAC. HSD and $\overline{SLDB}/\overline{SLDW}$ are discussed in the ACRTC User's Manual, and GMIC Data Sheet respectively.

Figure 15-18 illustrate video signal outputs for smooth scrolling vs frame buffer access in each mode. Video output start timing for display data is shifted corresponding to the shifted assertion of the HSD input. This video signal output is ANDed with the display timing signal ($\overline{DISP}$) and two-memory-cycle delayed (a signal indicating the output enable period for the video pins). Therefore, the video output signal of display data read from frame buffers by the first display amount. In the last display cycle of a raster, accessed display data output bits corresponding to the scrolling amount are displayed, and the remaining bits are removed.

Horizontal Zoom

Video signals for zooming are obtained when the period of the shift clock corresponding to the dot clock is extended by the shift clock enable (SCKE) input. The ACRTC specifies the zoom scale (HZ3-HZ0), and the GMIC outputs the SCKE control signal according to the specified zoom scale. SCKE is sent to the GVACs to implement zooming. Figures 15-17 show zoom display timing for each mode. In figure 15, quadruple zoom is performed by applying the shift clock enable (SCKE) once during the four-cycle dot clock (DOTCK).

Table 20. Horizontal Smooth Scroll Amount and $\overline{SLD}$ Cycle Count

MOD		Dot count for horizontal smooth scroll																Shift
1	0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	length
0	0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	32
1	0	0	1	2	3	4	5	6	7	Cannot be used								8
1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

MOD		Dot count for horizontal smooth schrool																Shift
1	0	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	length
0	0	Cannot be used																6
0	1	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
1	0	Cannot be used																8
1	1	Cannot be used																16

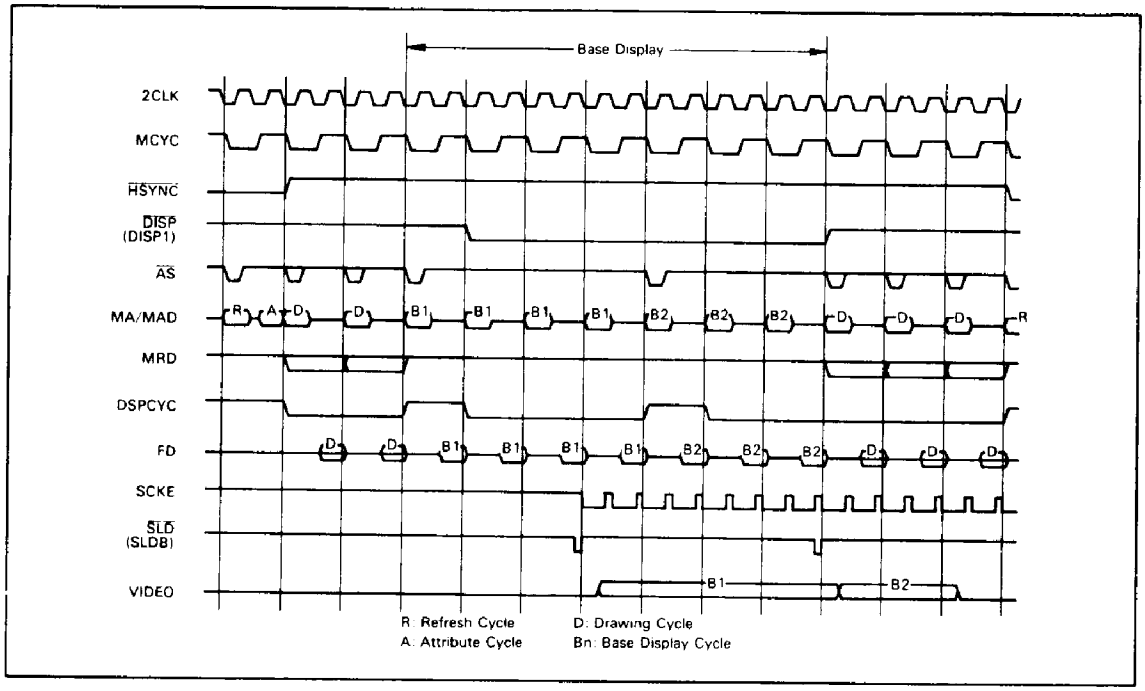

Figure 15. Zoom Display Timing (Single Access Mode, Quadruple Zoom)

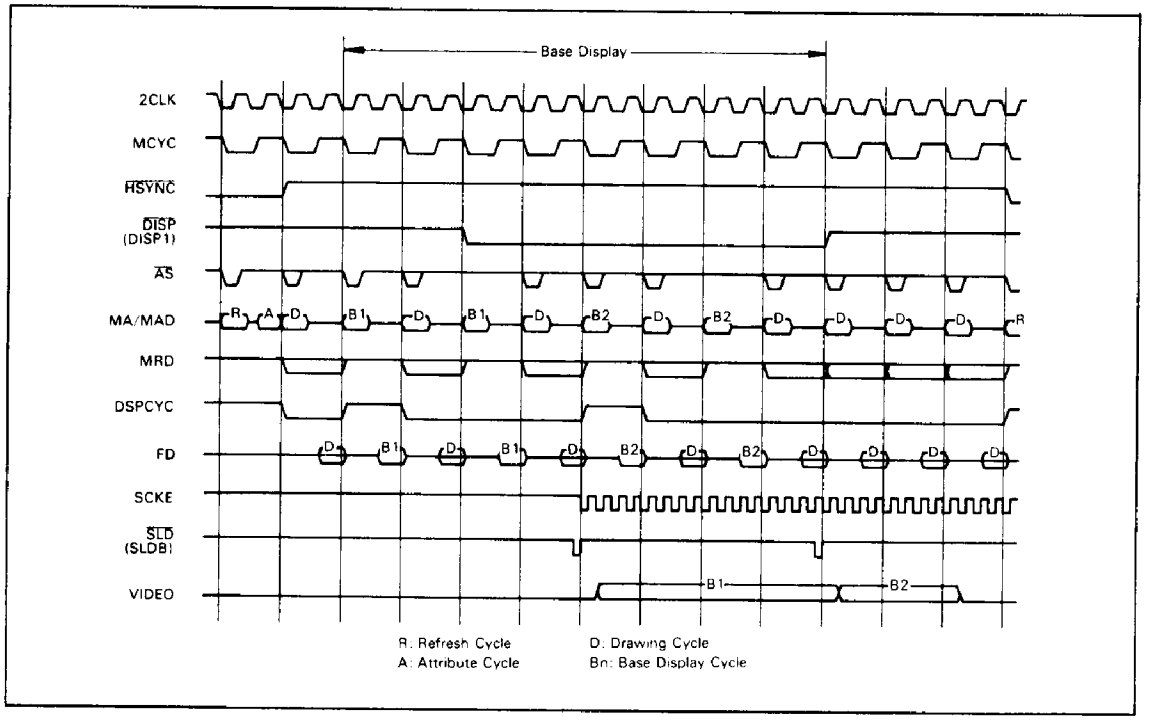

Figure 16. Zoom Display Timing (Dual Access Mode 0, Double Zoom)

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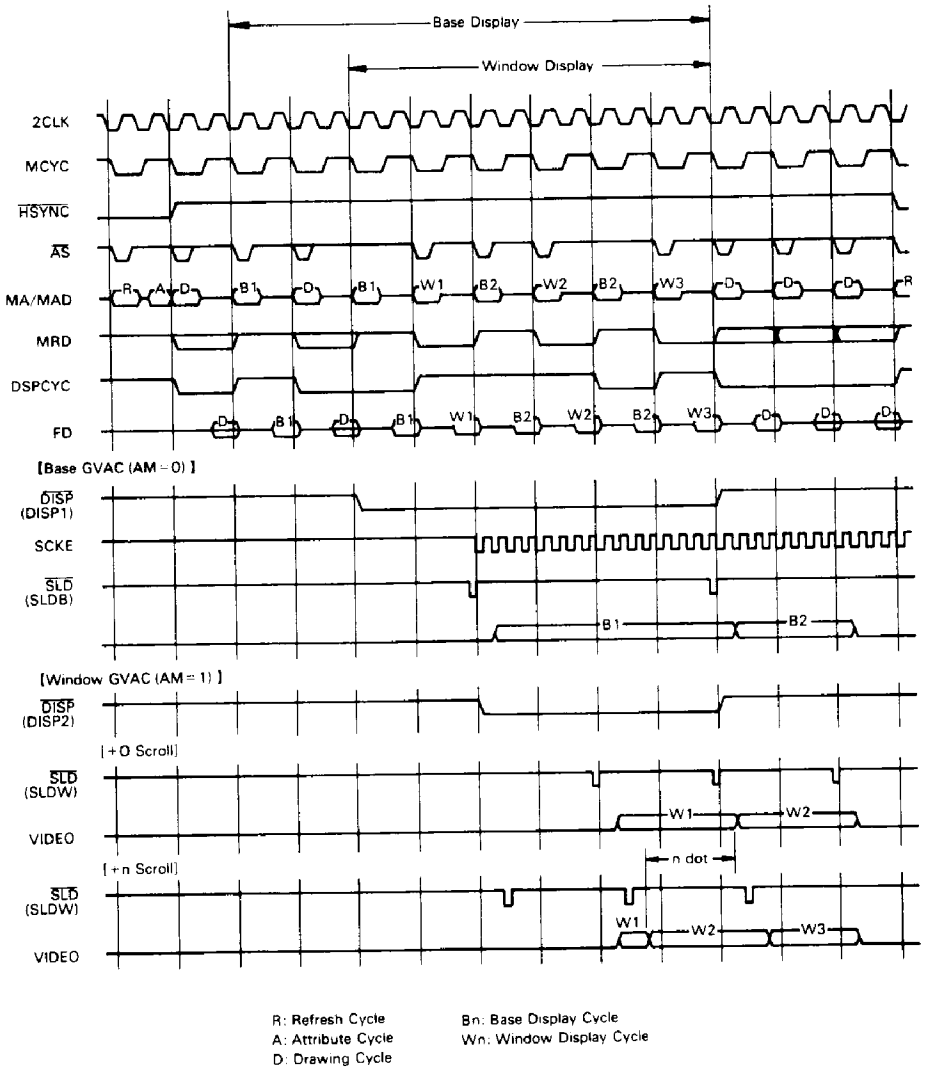

Figure 17. Zoom Display Timing (Dual Access Mode 1, Double Zoom)

Absolute Maximum Ratings (All voltages referenced to V_{SS} = 0 V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{in}	−0.3 to V_{CC} +0.3	V
Output voltage	V_{out}	5.5	V
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{str}	−55 to +150	°C

Notes: Using an LSI beyond its maximum ratings may result in its permanent destruction. LSI's should usually be operated under the recommended operating conditions. Exceeding any of these conditions may adversely affect its reliabity.

Recommended Operating Conditions (All voltages referenced to V_{SS} = 0 V)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Input voltage low	V_{IL}	0	—	0.7	V
Input voltage high	V_{IH}	2.2	—	V_{CC}	V
Operating temperature	T_{opr}	0	25	70	°C

Electrical Characteristics

DC Characteristics (V_{CC} = 5.0 V ± 5%, V_{SS} = 0 V, T_a = 0°C to +70°C, unless otherwise noted)

Item		Symbol	Min	Max	Unit	Test Condition
Input voltage high		V_{IH}	2.2	V_{CC}	V	
Input voltage low		V_{IL}	−0.3	0.7	V	
Input clamp voltage		V_I		−1.5	V	V_{CC} = 4.75 V, I_{in} = −18 mA
Output voltage high		V_{OH}	2.7		V	V_{CC} = 4.75 V, I_{OH} = −400 mA
Output voltage low		V_{OL}		0.5	V	V_{CC} = 4.75 V, I_{OL} = 8 mA
Input current high		I_{IH}		20	μA	V_{CC} = 5.25 V, V_I = 2.7 V
Input current low		I_{IL}		−400	μA	V_{CC} = 5.25 V, V_I = 0.4 V
High level output current		I_{CH}	—	100	μA	V_{CC} = 5.25 V, V_I = 5.5 V
Output short circuit current		I_{OS}	−40	−120	μA	V_{CC} = 5.25 V
Current consumption		I_{CC}		160	μA	V_{CC} = 5.25 V
Input capacitance		I_{in}		10	pF	
Off-state output current	D_7-D_0,	I_{OZH}		20	μA	V_{CC} = 5.25 V, V_O = 2.7 V
	FD_{31}-FD_0	I_{OZL}		−20	μA	V_{CC} = 5.25 V, V_O = 0.4 V

AC Characteristics (V_{CC} = 5.0 V ± 5%, V_{SS} = 0 V, T_a = 0°C to +70°C)

			32 MHz		48 MHz		64 MHz			
No	Item	Symbol	Min	Max	Min	Max	Min	Max	Unit	Figure
	DOTCK operation frequency	f		32		48		64	MHz	
①	DOTCK cycle time	t_C	31.3		20.8		15.6		ns	18
②	DOTCK high level pulse width	t_{HW}	12		9		6		ns	
③	DOTCK low level pulse width	t_{LW}	12		9		6		ns	
④	DOTCK rise time	t_R		5		5		5	ns	
⑤	DOTCK fall time	t_F		5		5		5	ns	
⑥	SCKE setup time	t_{SCKS}	6		2		0		ns	
⑦	SCKE hold time	t_{SCKH}	5		5		5		ns	
⑧	$\overline{SLD}$ setup time	t_{SLDS}	6		2		0		ns	
⑨	$\overline{SLD}$ hold time	t_{SLDH}	5		5		5		ns	
⑩	VIDEO delay time	t_{VD}	3	24	3	17	3	14	ns	
⑪	2CLK setup time	t_{2CKS}	6		2		0		ns	19-21
⑫	MCYC setup time	t_{MCYCS}	30		30		30		ns	
⑬	MCYC hold time	t_{MCYCH}	0		0		0		ns	
⑭	FD threelstate recovery time	t_{FDR}	5		5		5		ns	20
⑮	FD setup time	t_{FDS}	30		30		30		ns	21
⑯	FD hold time	t_{FDH}	5		5		5		ns	

AC Characteristics (cont)

No	Item	Symbol	32 MHz Min	32 MHz Max	48 MHz Min	48 MHz Max	64 MHz Min	64 MHz Max	Unit	Figure
⑰	D three state recovery time	t_{DR}	5		5		5		ns	19
⑱	D hold time	t_{DH}	5		5		5		ns	
⑲	FD delay time from D	t_{FDDLY}		30		30		18	ns	20
⑳	D delay time from FD	t_{DDLY}		30		30		18	ns	19
㉑	SEL setup time	t_{SELS}	10		10		10		ns	19, 20
㉒	SEL hold time	t_{SELH}	5		5		5		ns	
㉓	DSPCYC setup time	t_{DSPS}	20		20		20		ns	19-21
㉔	DSPCYC hold time	t_{DSPH}	5		5		5		ns	
㉕	MRD setup	t_{MRDS}	20		20		20		ns	
㉖	MRD hold time	t_{MRDH}	10		10		10		ns	
㉗	$\overline{DISP}$ setup time	t_{DISPS}	20		20		20		ns	21

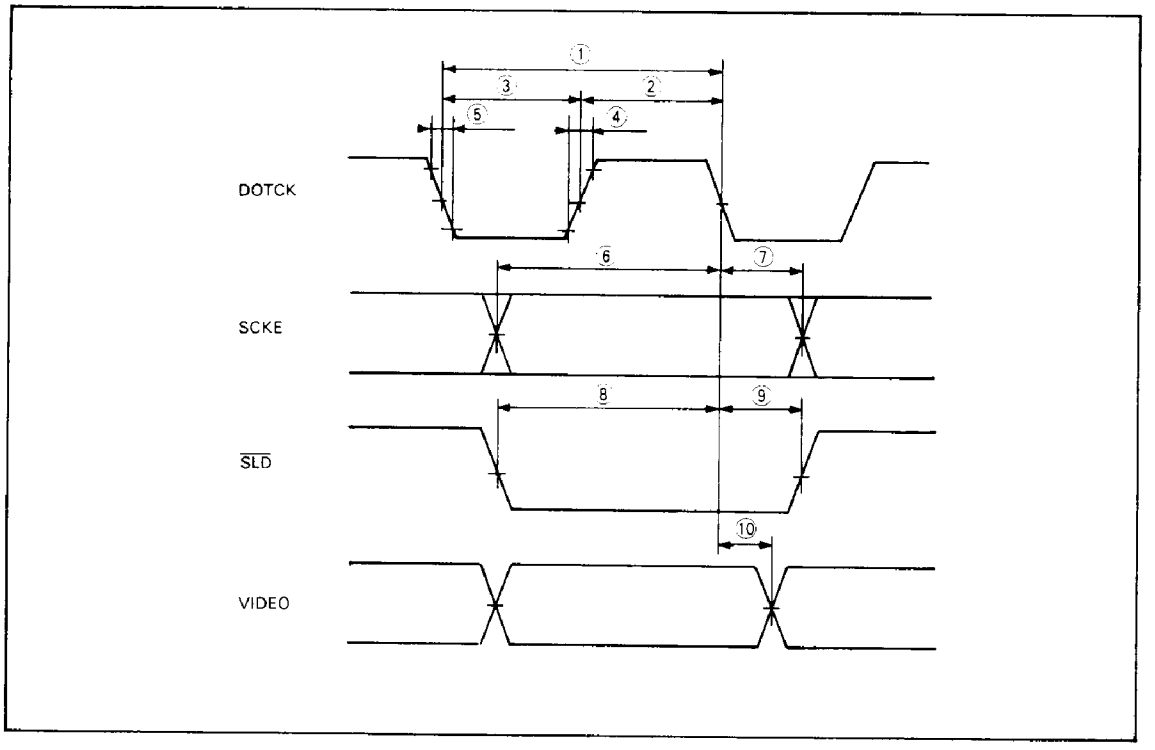

Figure 18. Dot Clock

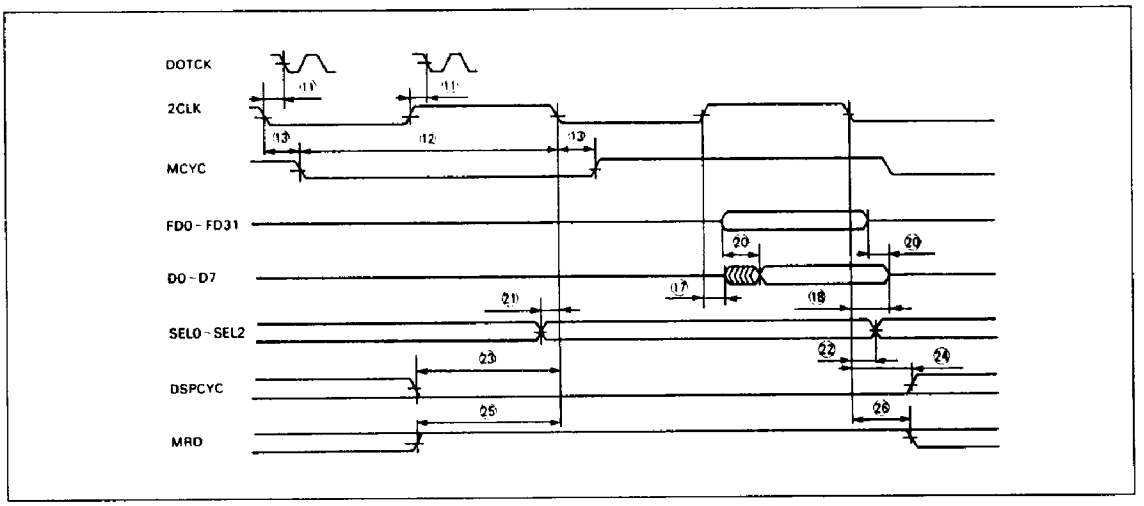

Figure 19. Drawing Read Cycle

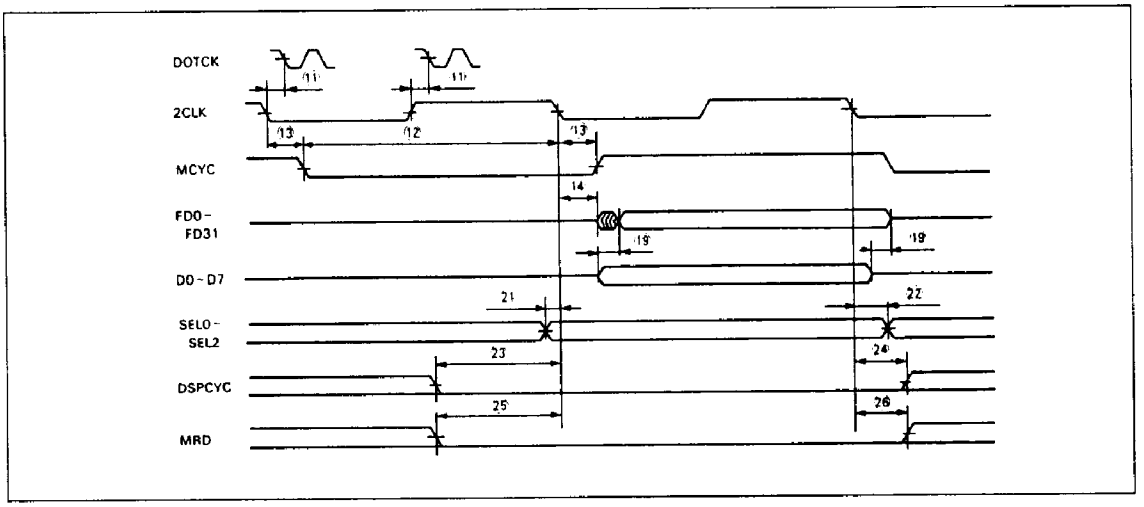

Figure 20. Drawing Write Cycle

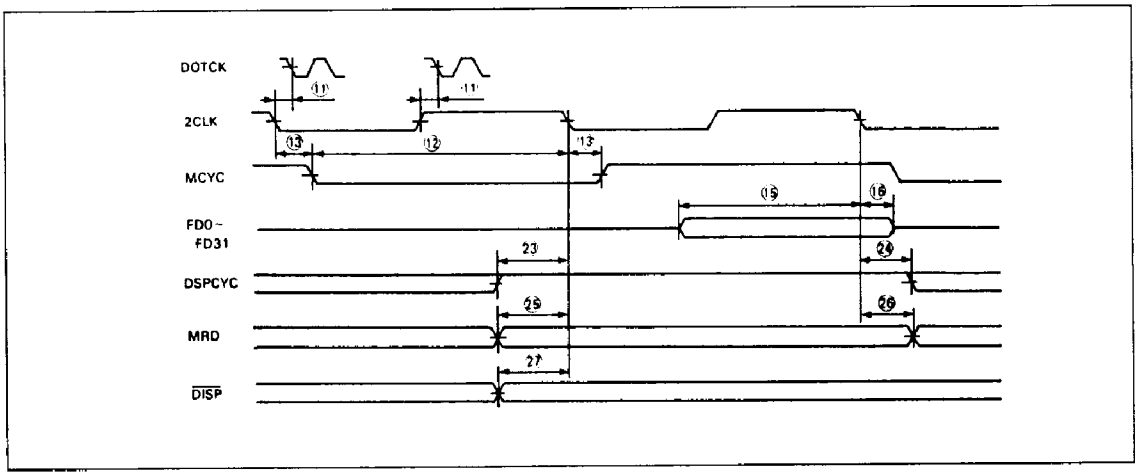

Figure 21. Display Cycle